What is Claimed is:

1.   An apparatus that provides dynamic phase alignment for a multi-channel communications protocol comprising:

     a phase-locked loop circuit that

5   receives as input a clock and is operative to generate a plurality of clock phases; and

     a dynamic phase alignment circuit associated with a channel in the multi-channel communications protocol that receives as input a data

10 signal and the plurality of clock phases, wherein the dynamic phase alignment circuit is operative to select a clock phase from the plurality of clock phases from which to align the data signal for output to the channel.

2.   The apparatus of claim 1 wherein the plurality of clock phases has a same period as the period of the clock and is equally spaced apart in phase.

3.   The apparatus of claim 1 wherein the dynamic phase alignment circuit further comprises a multi-phase sampling serializer-deserializer circuit operative to:

5   sample the data signal at each of the plurality of clock phases;

     align the data signal at each of the plurality of clock phases to one of the plurality of clock phases; and

10   deserialize the data signal to form an aligned byte of data associated with each of the plurality of clock phases.

4.   The apparatus of claim 3 further comprising an active alignment selector circuit coupled to the output of the multi-phase sampling serializer-deserializer circuit and operative to select one of the plurality of clock phases.

5.   The apparatus of claim 4 wherein the active alignment selector circuit is operative to select a same clock phase as a previously selected clock phase.

6.   The apparatus of claim 4 wherein the active alignment selector circuit is operative to select a clock phase that is adjacent in phase to a previously selected clock phase.

7.   The apparatus of claim 4 wherein the active alignment selector circuit is operative to select a clock phase that is non-adjacent in phase to a previously selected clock phase.

8.   The apparatus of claim 4 wherein the active alignment selector circuit further comprises:
        an edge detector circuit that accepts as input a bit value in a same bit location for each aligned byte of data and is operative to indicate a difference between bit values associated with adjacent clock phases; and
        a lookup table that accepts as input the output of the edge detector and the output of the lookup table, wherein the lookup table is operative to output select signals corresponding to one of the plurality of clock phases.

9.　The apparatus of claim 8 wherein the edge detector circuit further comprises a plurality of XOR gates, wherein each of the plurality of XOR gates receives as input two bit values associated with

5　adjacent clock phases.

10.　The apparatus of claim 8 wherein the active alignment selector circuit further comprises a filter that accepts as input the select signals from the lookup table.

11.　The apparatus of claim 4 further comprising a multiplexer coupled to the output of the multi-phase sampling serializer-deserializer circuit and the active alignment selector circuit, wherein the

5　multiplexer is operative to select the aligned byte associated with the selected one of the plurality of clock phases.

12.　The apparatus of claim 1 wherein the dynamic phase alignment circuit is further operative to perform clock recovery and wherein the data signal received as input a clock embedded in the data signals.

13.　The apparatus of claim 1 wherein the apparatus is a programmable logic resource.

14.　The apparatus of claim 1 wherein the apparatus is an application-specific standard product.

15.　The apparatus of claim 1 wherein the apparatus is an application-specific integrated circuit.

16. A programmable logic resource comprising:

programmable logic resource core circuitry; and

5   an intellectual property block that supports a multi-channel communications protocol and is coupled to the programmable logic resource core circuitry, wherein the intellectual property block comprises circuitry that accepts as input a clock and

10   data signals from the programmable logic resource core circuitry and selects a phase of the clock from which to align the data signals for output to each channel in the intellectual property block.

17. The programmable logic resource of claim 16 wherein the circuitry further comprises:

a phase-locked loop circuit that receives as input the clock and is operative to

5   generate a plurality of clock phases;

a dynamic phase alignment circuit associated with each channel in the intellectual property block that receives as input respective data signals and the plurality of clock phases, wherein each

10   dynamic phase alignment circuit is operative to select a clock phase from the plurality of clock phases from which to align the respective data signals for output to each channel.

18. A digital processing system comprising:
processing circuitry;
a memory coupled to the processing circuitry; and

5   the programmable logic resource as

defined in claim 16 coupled to the processing circuitry and the memory.

19. A printed circuit board on which is mounted the programmable logic resource as defined in claim 16.

20. The printed circuit board defined in claim 19 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic resource.

21. The printed circuit board defined in claim 19 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable

5   logic resource.

22. A method for providing dynamic phase alignment for a multi-channel communications protocol comprising:

receiving as input a clock and
5   generating a plurality of clock phases based on the clock;

sampling input data at each of the plurality of clock phases;

determining which one of the plurality
10   of clock phases from which to align the input data for output to a channel in the multi-channel communications protocol; and

sending the input data sampled at the determined one of the plurality of clock phases as
15   output to the channel.

23. The method of claim 22 wherein the sampling further comprises:

aligning the input data at each of the plurality of clock phases to one of the plurality of

5   clock phases; and

deserializing the input data at each of the plurality of clock phases to generate an aligned byte of data associated with each of the plurality of clock phases.

24. The method of claim 23 wherein the determining further comprises:

selecting a bit value in a same bit location for each aligned byte of data;

5   comparing pairs of bit values associated with adjacent clock phases; and

for each pair of bit values associated with adjacent clock phases:

sending a first output when the bit

10   values are different, and

sending a second output when the bit values are the same.

25. The method of claim 24 further comprising determining an optimal clock phase from the plurality of clock phases based on the output for each pair of bit values.

26. The method of claim 25 wherein the determined one of the plurality of clock phases is the optimal clock phase.

27. The method of claim 25 wherein the determined one of the plurality of clock phases is a

clock phase that is immediately adjacent in phase to a previously selected clock phase and that is one phase

5   closer to the optimal clock phase.